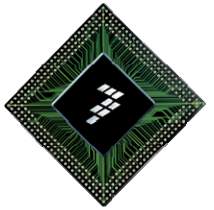
WIND RIVER

Regional Developer Conference

December 2007



Multi-Core Technology Direction

YK Ho and Jeffrey Ho

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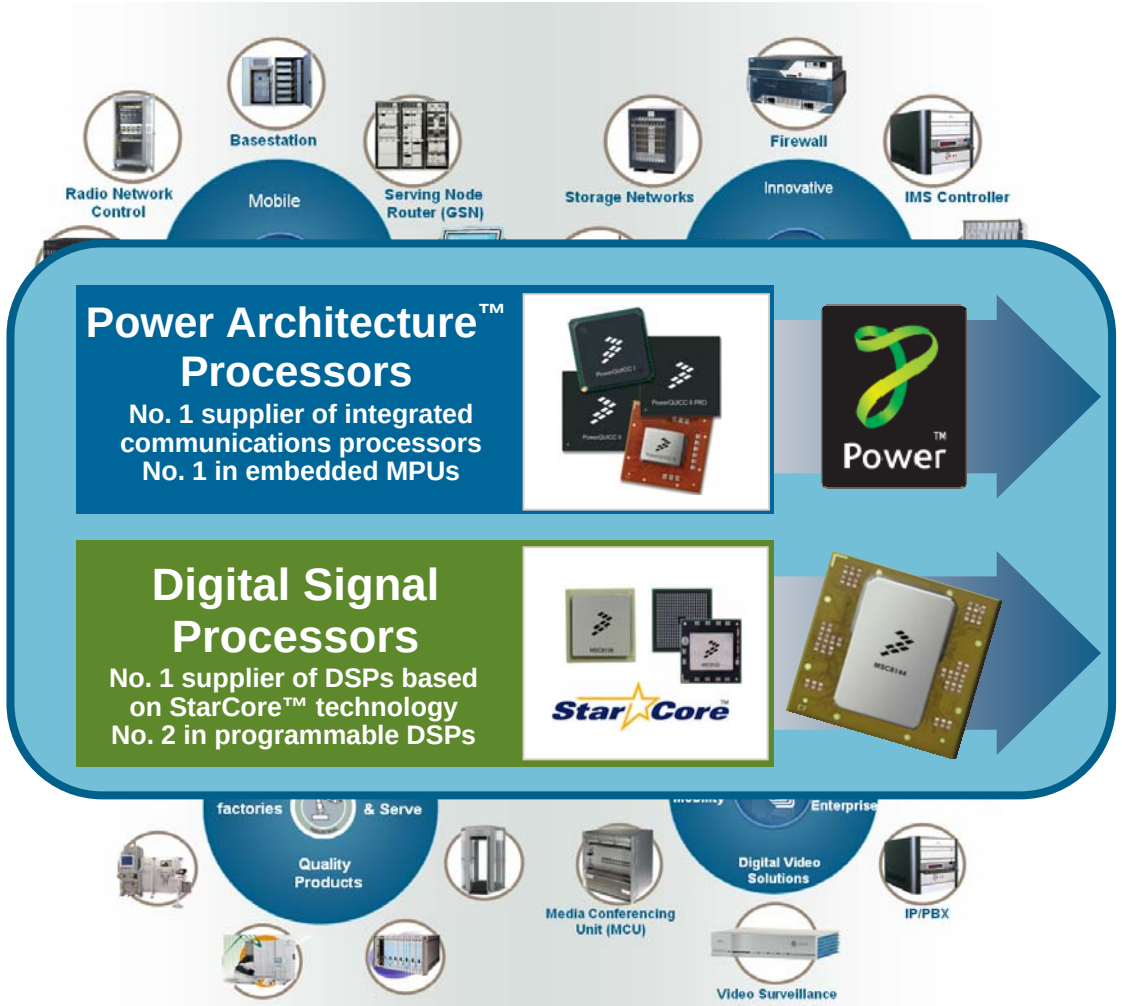
Networking Leadership Since 1995



▸Integrated Networking

- QUICC Engine™
- GbE, PCI-Express, Serial RapidIO

▸Power Efficient, Real-time Embedded

- Low-power Cores and I/Os
- Protocol integration

▸Multi-layer Security

- Authentication, IPSec, IPS/IDS

▸Scalable Service Processing

- Up to 1.5 GHz + Multi-Core
- Heterogeneous

▸Application Acceleration

- Deep-packet-inspection
- Pattern-matching
- Multi-Core aware

▸Content Processing

- HD Video Transcoding
- Highest Performing Multi-Core DSP

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FTF News Highlights

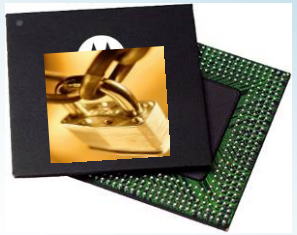
Process Technology Development

- Collaboration with IBM Alliance for 45-nm, 32-nm, Bulk-CMOS, and SOI
- 45-nm manufacturing agreement with Chartered Semiconductor
- Advanced R&D for 22-nm and beyond with IBM Alliance

Chartered semiconductor manufacturing IBM

Freescale Bundles Security Stacks

- Enables faster time to market by bundling an optimized secure protocol stack with all MPC8xxxE devices.



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Freescale Opens Licensing of Power Architecture™ for e200 core family

- Applicable to full range of automotive, industrial control, robotics, consumer & many other networking applications

IPextreme

Freescale Announces Multi-core Simulator Platform

- Enables pre-silicon software architecture assessment and what-if analysis.
- Hybrid simulator supports functional & cycle-accurate simulation for productivity and predictivity.

SIMICS MODEL BUILDER virtutech

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System Level Challenges –
Enabling Our Customers to Make Their Products More Compelling

- Open, standards-based
- Pervasive connectivity options
- Flexible and Extensible
- Delivery of intelligent services
- Application-aware security
- Improved ability to collaborate

Freescale's Strategic Objective:
Provide an innovative, flexible, and open networking platform solution to enable our customers to realize value, leadership, and loyalty for their products

Silicon ● Tools ● Run-time SW ● Boards ● Reference Designs ● Etc.

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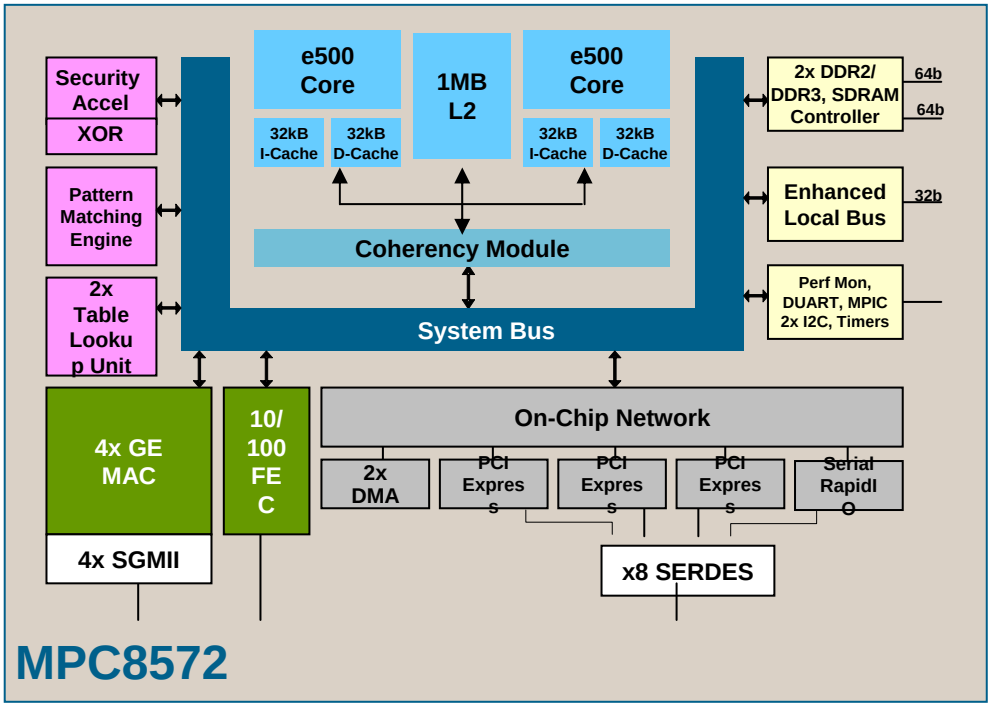
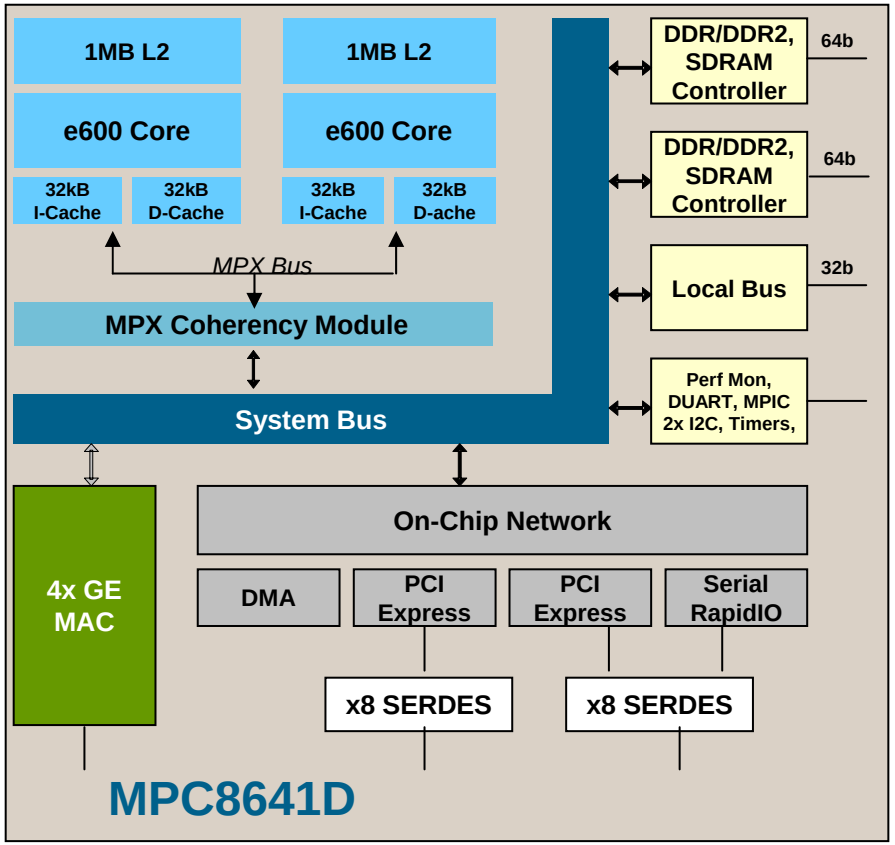
Current Power Architecture Multicore Block Diagrams





Two powerful alternatives with state of the art processing performance.
Highly integrated SoC with optimized coherent memory controllers

Samples Available - Now

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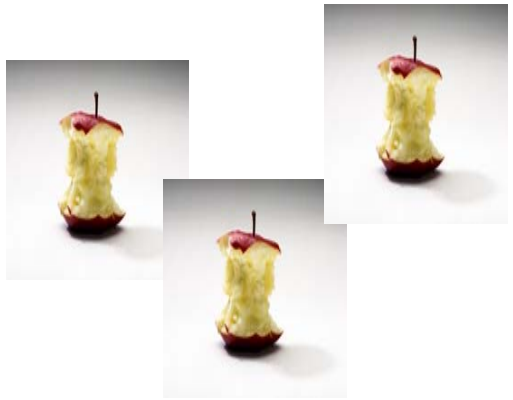
Hot "news" in the embedded world

Technology Trends

- Multiple cores are tried and true, but Multi-core is new
- The installed base of single core devices have designers looking for the right combination of technology
- Built-in expectations of “Doubling” to keep up with the growth, may not be enough



Market Trends

- Every network connection matters
- Explosive rate of content growth
- New applications require efficient integration and security
- Evolving collaboration models create new user environments

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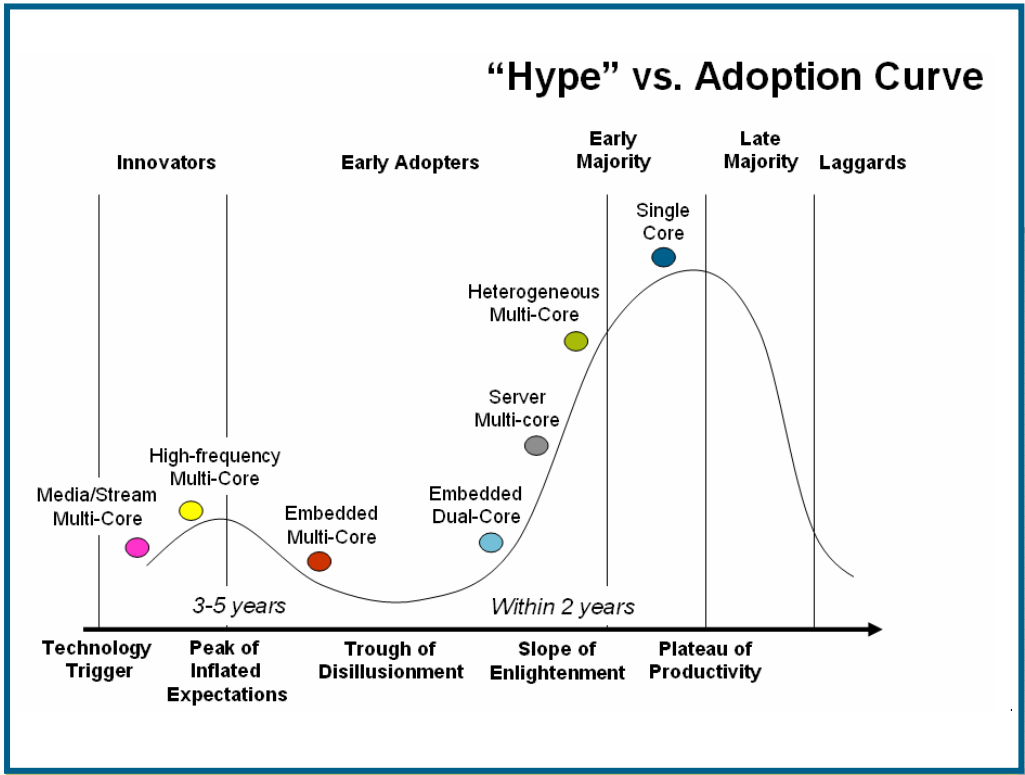
We're at an Inflection Point

►The installed base of communications processors are still largely single-core devices but systems designers desire to leverage dual-core and then multi-core architectures to solve their next-generation challenges.



►However, first-generation multi-core platforms are seeing mixed reviews.

- "That's too high-powered for my application."
- "How do I port my legacy application?"
- "I can't tell what my performance will be."
- "How do I partition my application?"
- "Why don't I see n-times higher performance?"

Silicon Challenges:

- Application complexity and flexibility drive scalable, software-based solutions.
- Balanced architectures must deliver performance "greater than Moore's law" within system power budgets.
- Existing code must be leveraged to new architectures to preserve familiar service experiences.

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What's the News?

It's a smarter approach to multi-core.
Freescale's Multi-Core Platform

►**Innovative Multi-Core Microarchitecture** for unprecedented computing efficiency, performance and scalability.

- On-chip Fabric
- Back-side Cache per CPU Core
- On-Demand Application Acceleration

►**Multi-Core Simulation Environment** for accurate, fast code development and debugging.

- Fully tap the capabilities of the multi-core platform
- Debug software not hardware
- Dynamic, real-time debug with non-intrusive capture

►**45-nm Process Technology** for industry-leading power-to-performance solution.

- Provides highest instructions-per-cycle (IPC) and frequency for given milliwatt/area

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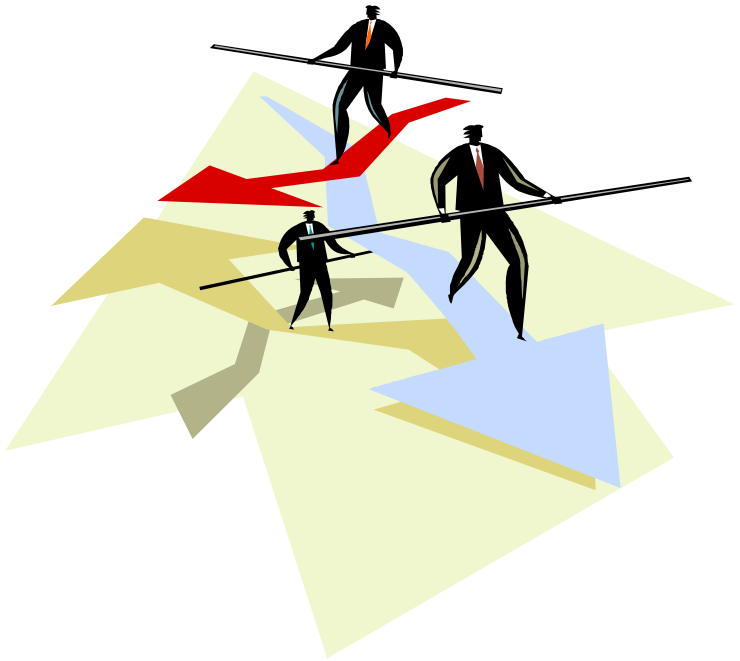
Purposeful Approach to Multicore

- Balance of system elements to find right combinations:
  - ✓**Cores**
  - ✓**Memories**
  - ✓**Peripherals**
  - ✓**Software environment**
  - ✓**Partners**



- Balance with Freescale Multicore experience

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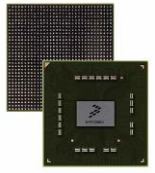
Power Architecture Multi-Core Solutions from Freescale

- **MPC51xx Power Architecture™ MobileGT family**
  - e300 Power Architecture™ core + graphics core + audio core
- **MPC5510 Power Architecture™ automotive microcontrollers**
  - e200z1 + optional e200z0 Power Architecture cores
- **PowerQUICC + QUICC Engine**
  - Power Architecture™ Core + 2 RISC cores for protocol interworking
- **PowerQUICC + Content Processing**
  - Dual e500 Power Architecture™ cores + acceleration IP
- **MPC8641D Host Processor**
  - Dual e600 Power Architecture™ cores
- **GPON processor**
  - Power Architecture core + StarCore® DSP core



- Freescale Power Architecture SoCs use a combination of standard CPU processing mixed with a variety of co-processing options tailored to specific market needs.
- These heterogeneous processing solutions may integrate
  - One or more Power Architecture cores (homogeneous and heterogeneous multi-core configurations)
  - On-chip co-processors
  - Flexible hardware acceleration
- Freescale's new Multi-core Platform establishes a common architecture for communications processing solutions moving forward.

- **NEW Multi-core Communications Platform**
  - 2 to >32 Power Architecture cores (can mix and match) + on-demand acceleration

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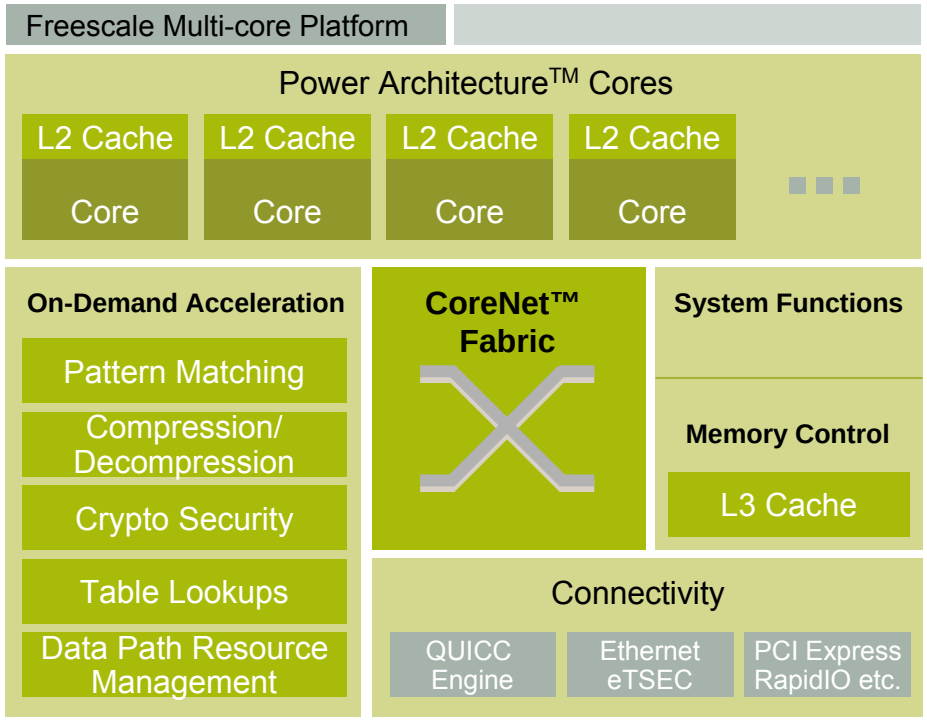
The New Multi-Core Platform Details

The New Multi-Core Platform



- Introducing **CoreNet Fabric** for concurrent, non-blocking, hardware-based cache-coherent platform connectivity
  - Eliminates shared bus contention and supports dramatically higher address issue bandwidth to “feed” multiple CPU cores
  - Scales to support more than 32 cores
  - Supports heterogeneous cores
- Supporting an Innovative **Tri-level Cache Hierarchy**
  - Heterogeneous Power Architecture™ cores with L1 I + D and unified back-side L2 caches
  - Supports multiple L3 shared caches
  - Supports multiple memory controllers
- Including **On-demand Application Acceleration**
  - Expected to enable 2-3 times improved system performance

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Cache and Memory Subsystem

- Performance engineered Tri-Level cache hierarchy
  - Heterogeneous Power Architecture™ cores separate L1 Instruction and Data caches
- Unified back-side L2 cache per core
  - Optimal sizing for application performance
  - Minimizes access latency
- Supports multiple L3 shared caches
  - Flexible cache partitioning on per core basis
  - Cache header stash
- Multiple Memory Controllers
  - Support for DDR2 and DDR3 SDRAM

Platform options for multicore

Integrated I/O Interface Technology

- DUART, I2C, SPI, LPC
- 10/100/1000 Ethernet
  - SGMII, IEEE 1588, FIFO
- 10G Ethernet
  - XAUI
- PCI/PCI-X
- sRIO
- PCI-Express
- Local Bus
  - NOR/NAND Flash
- USB 2.0
- SATA

On Demand Acceleration

- **Packet Processing**
- SEC Security
  - Look-aside protocol aware crypto-acceleration
- Pattern Matching Engine
  - Look-aside *regex* pattern matching
- Table Look-up Unit
  - Look aside offload for packet classification
- **Data Path Resource Management**
- Data Buffer and Queue Management
- Intra-core Message Passing

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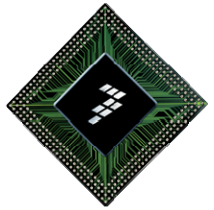
Software Considerations for Multicore



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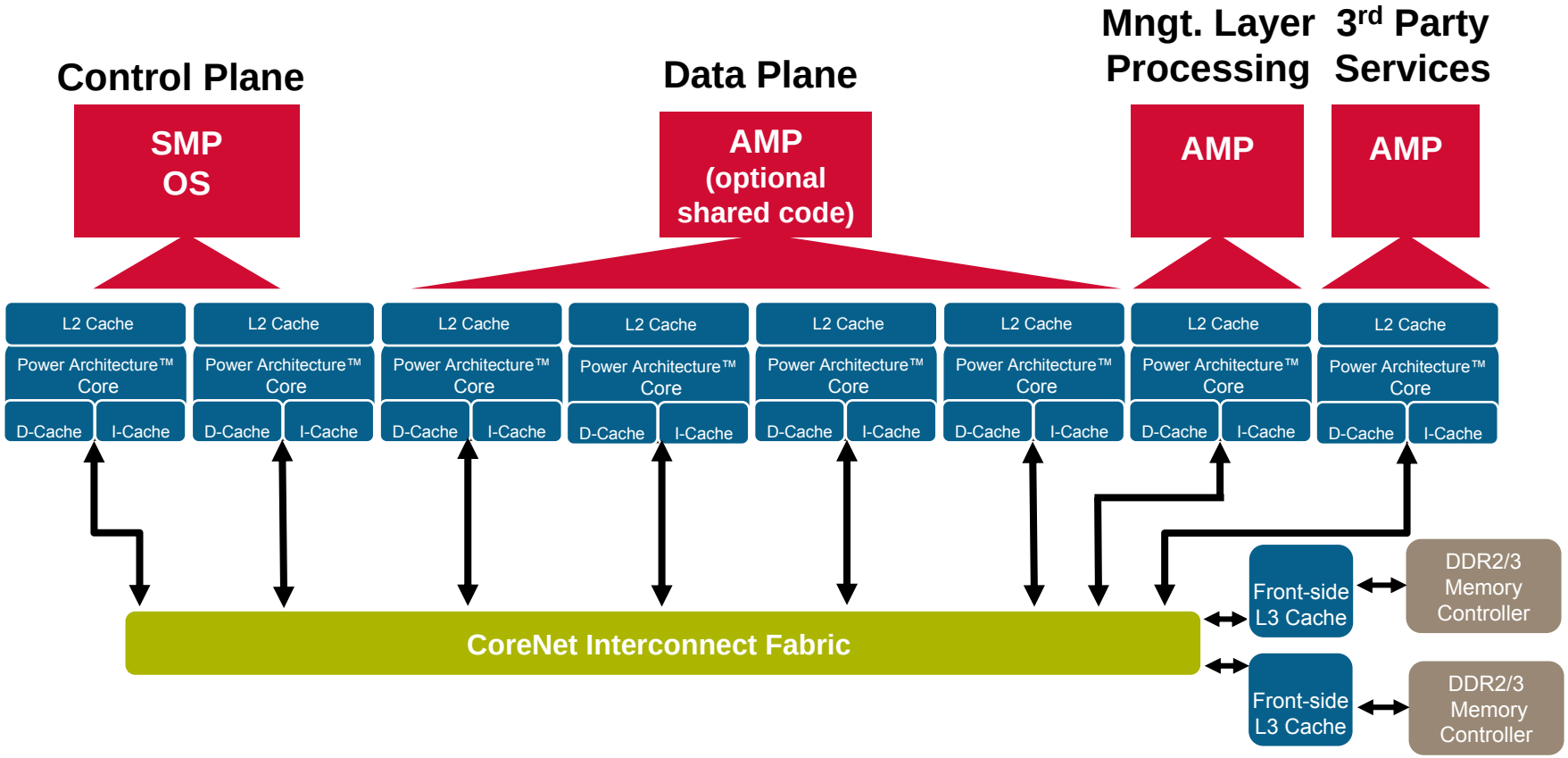
Software development Challenges

- Application complexity and flexibility drives scalable, software-based solutions
- Partitioning and code parallelism
- Balanced architectures must deliver performance “greater than Moore’s law” within system power budgets.
- SMP vs. AMP which is right for the application
- Maturity of development tools
- Debug capability and tools

Multi-Core System Usage Models

Flexible choice of OS model on cores—any combination of SMP/AMP.

IP Services Router example (mixed control and data plane mapping):



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Multi-Core Development Environment

- **Virtualization enables partitioning of resources among System Classes**
  - Core, Memory, I/O, Accelerators
- **Supports flexible mix of SMP/AMP (control plane, data plane) as well as 3rd party services**
  - On-chip fabric enables scalable cache-coherent memory access with isolation and protection
- **Multi-Core Diagnostics supporting trace, event, and application performance analysis**
- **Hybrid simulation environment enables migration and partitioning of OSs and applications onto a full multi-core system**
  - Enables fast, accurate performance prediction and software optimization

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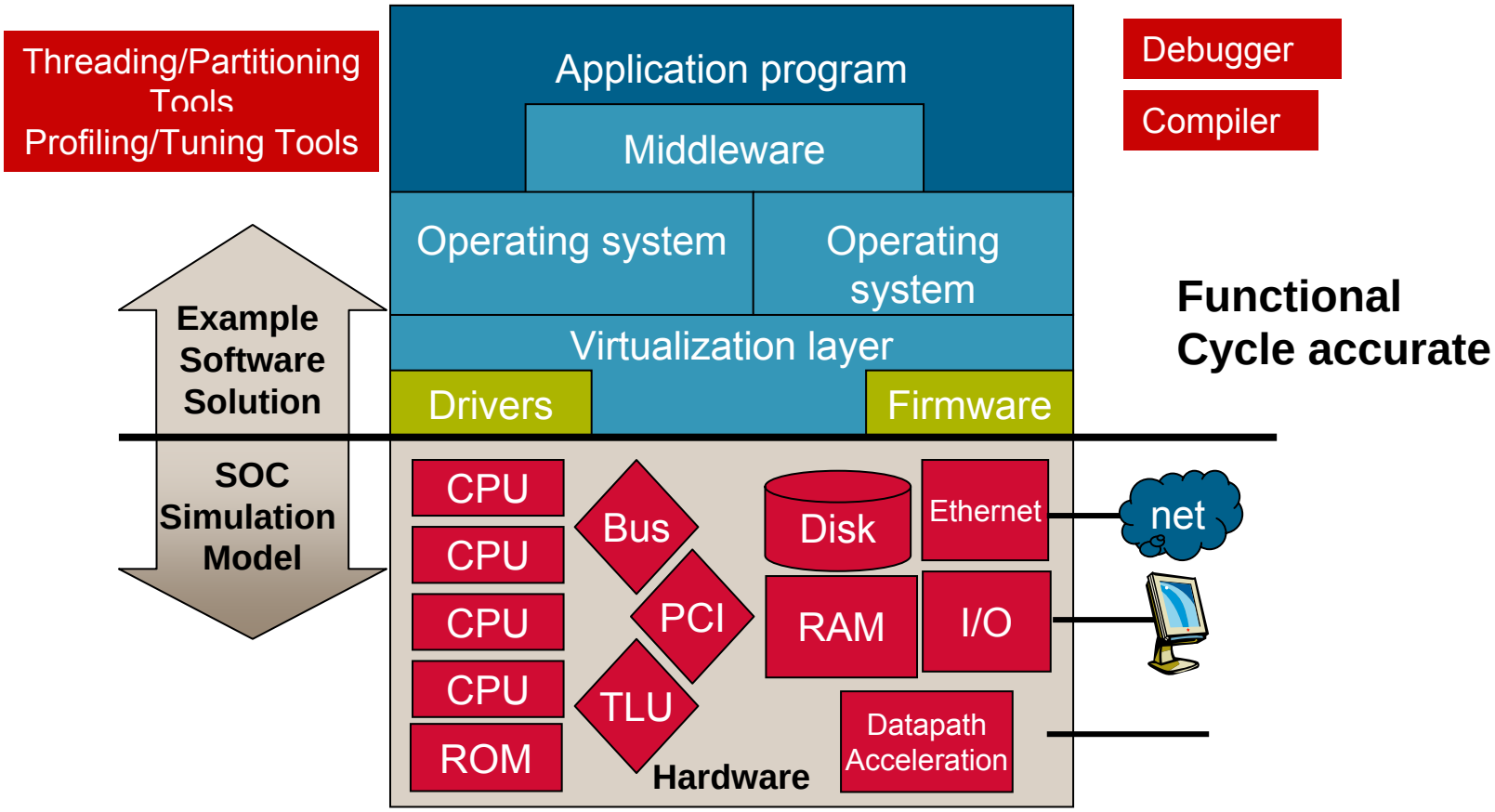
Virtual Environment Simulating Hardware and Software

Multi-Phased Approach

Distinctive Competence

Solutions bring value



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45-nm Process: Technology is a key enabling force

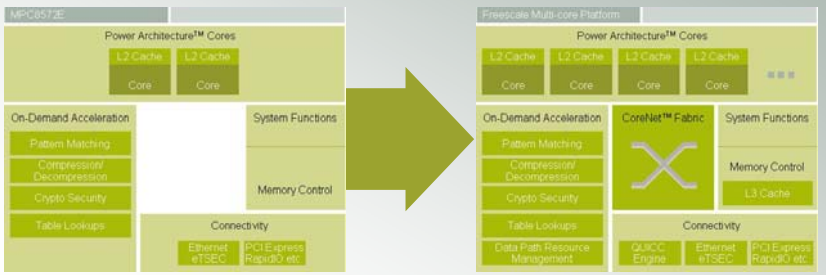
Process Technology Development

- Collaboration with IBM Alliance for 45-nm, 32-nm, Bulk-CMOS, and SOI
- 45-nm manufacturing agreement with Chartered Semiconductor
- Advanced R&D for 22-nm and beyond with IBM Alliance

Chartered semiconductor manufacturing IBM

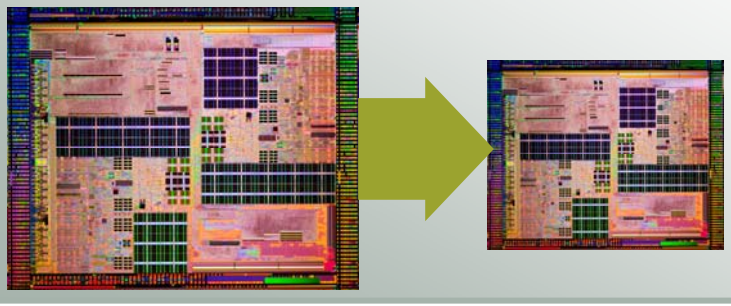
45-nm Integration Enabler

- More functionality within the same die area to enable improved system performance



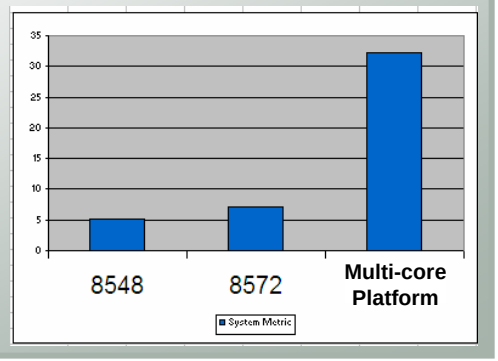
45-nm Energy Advantages

- Same functionality delivered today in 90-nm will achieve 50% die size reduction and 50% lower power in 45-nm



45-nm Performance Leap

- Multi-Core Platform in 45-nm Process Technology delivers over 4x improvement in System Performance



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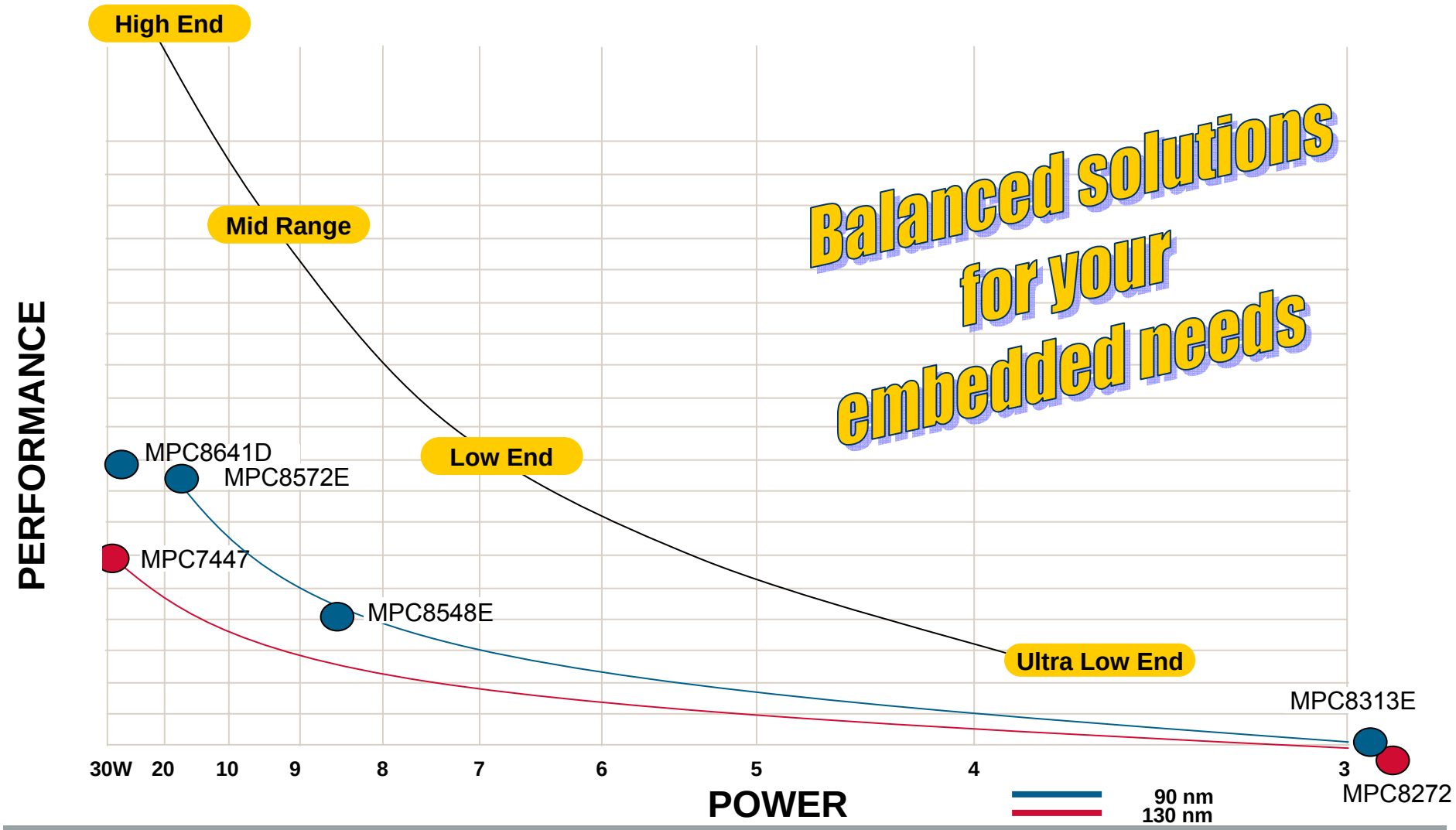
Freescale's New Multi-Core Communications Platforms



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Freescale Multi-Core Platform Will Deliver Scalable, Software-Based Solutions that Preserve and Extend the User Experience Through New Services

High-performance Multi-core	 Metro Carrier Edge Router	 IMS Controller	 Radio Network Control	 Serving Node Router (GSN)
Mid-range Multi-core	 Converged Media Gateway	 SSL, IPSec, Firewall	 Access Gateway	
Low-end Multi-core	 Unified Threat Management	 VoIP Carrier-Class Media Gateway	 Wireless Media Gateways	 Basestation
Ultra Low-end Multi-core	 Integrated Services Routers	 Network Attached Storage	 Home Media Hub	

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Making Better Networks

World Class Alliances
Strategic Technology Collaboration

freescale semiconductor ™ | Power | IBM

e200 e300 e500 e600 e700

SOC integrated devices
Embedded power budgets
Networking life cycles
Networking/security IP
Content Aware Packet Processing

Development and Production Systems
in Standard Industry Form Factors

RadiSys. THE POWER OF WE | FLEXTRONICS | Computer Systems, Inc. MERCURY

EMBEDDEDPLANET | CELESTICA | freescale semiconductor | kontron

Responsivity
Adaptive
Change

Productive
Hardware
Enablement

IP Services

Productive
Secure
Networks

Collaboration
Software
Partners

WIND RIVER | mocana | ClamAV | SNORT.ORG | JUNGO | Arabella SOFTWARE | SpamAssassin | KASPERSKY lab

QNX SOFTWARE SYSTEMS | Linux | Green Hills SOFTWARE, INC. | Mentor Graphics | WIND RIVER | montavista | CodeWarrior

Optimize Application Specific Stacks for Continual Improvement in Network Security Solutions

Value Partners: Enable Faster Time to Market and Longer Time in Market

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Multicore Technology Direction Summary

- **An SoC platform influenced by multiple generations of embedded networking leadership.**
- **The Freescale Multi-core Platform unleashes the system performance potential of multi-core microarchitectures.**
  - Fabric vs. shared bus
  - Three-level cache hierarchy with private L2 cache per CPU core
  - On-demand application acceleration off-load
  - Scalable beyond 32 Power Architecture cores – supports heterogeneous cores
  - 45-nm process technology enables delivery within power budgets
- **Advanced simulation tools take multi-core programming to a new level (start today!).**
  - MPC8572 and its simulation model available today. This platform closely mirrors the first Multi-core Platform implementations.
  - Hybrid simulation environment supporting the new Multi-core Platform architecture
- **Comprehensive roadmap of products to be based on the Multi-core Platform, the first of which to hit the market in late 2008.**


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